TEMPERATURE AND BIAS EFFECTS in HIGH RESISTIVITY SILICON SUBSTRATES

Adolfo C. Reyes[1], Samir M. El-Ghazaly[2], Steve Dorn[1], and Michael Dydyk[3]

[1]C.P.L., S.P.S., Motorola, Inc., MD: EL720, 2100 E. Elliot Rd., Tempe, Arizona 85284
[2]Department of Electrical Engineering, Arizona State University, Tempe, Arizona 85287-5706
[3]G.S.T.G., Motorola, Inc., MD: R-2213, 8200 E. Roosevelt, Scottsdale, Arizona 85252

ABSTRACT

The purpose of this paper is to report the results of studies dealing with the impact of temperature and DC bias on low-cost low loss high resistivity (HR) Si substrate. Measured results show that microwave performance of a coplanar transmission lines and a meander inductive structure realized on HR Si are not affected by applied DC bias from -10 V to 10 V in the temperature range from -50 °C to 50 °C. Furthermore, measured results demonstrate that the losses of the structures under study on HR Si are comparable to the losses of similar structures on semi-insulating (SI) GaAs up to 100 °C.

INTRODUCTION

It was demonstrated in [1] that low cost HR Si with resistivities greater than 3 k Ω-cm can be used as a microwave substrate. The comparative experiments in [1] were carried out at 25 °C and zero DC bias on coplanar waveguides (CPW) and on inductive coplanar structures like meanders and single layer spiral inductors. However, results reported in [2] indicate that the attenuation of a microstrip transmission line on HR Si is dependent on the applied DC bias. Also, Si has a lower band gap than that of GaAs which make Si more sensitive to temperature. Practical application of integrated circuits requires the consideration of a wide temperature range and a wide DC bias range. Therefore, there is a need to investigate the practical application of the coplanar structures on HR microwave Si substrate through temperature and DC bias studies as functions of frequency.

In this paper, the comparative study in [1] is extended to include temperature and DC bias effects. Measurements show that DC bias has no effect on the microwave signal properties of the CPW and the meander structures up to 50 °C. Distinct DC bias effects are reported at 150 °C in both CPW and meander structures. Furthermore, the measured losses of the coplanar structure under study on HR Si are comparable to the measured losses of similar structures on SI GaAs up to 100 °C. Also, measurements indicate that the ohmic dielectric losses of the HR Si become the dominant loss mechanism at 150 °C on both coplanar structures under study due to the increase of intrinsic carriers..

DESCRIPTION OF THE EXPERIMENT

Measurements were taken on wafer using: 1) HP 8510C Vector Network Analyzer; 2) Cascade Microtech™ Summit 12651 Thermal Probing System; 3) Cascade Microtech™ high frequency ground-signal-ground coplanar probes; 4) LRM calibration technique to the probe tips at each temperature setting [3]; and, 5) a 1.59 mm quartz plate placed between the probe chuck and the sample. The quartz plate was used to remove the higher order modes of propagation produced by the presence of the probe chuck on the device under test and to electrically isolate the back of the H.R. Si wafer. The temperature setting used were: 150, 100, 50, 25, 0 -25, and -50 °C.

At each temperature setting, the DC bias was applied to the devices fabricated on the HR Si. The voltage was varied as follows: 10, 6, 3, 1.5, 0, -1.5, -3, -6, and -10 volts. The DC bias was applied to the coplanar structures through port 1 of the Vector Network Analyzer.

ANALYSIS OF RESULTS

Fig. 1. shows the measured losses of the of the CPW on HR Si, SI GaAs, and quartz as a function of frequency at 25 °C at zero DC bias. Fig. 1 is representative of the loss behavior of the CPW on the three substrates under study at zero

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DC bias at temperatures of -50 °C, -25 °C, 0 °C, and 50 °C. Below 3 GHz, the CPW on HR Si shows higher losses than that of the CPW on SI GaAs due to the effective (surface and bulk) ohmic loss of the HR Si. As the frequency increases, the impact of the ohmic loss on the total attenuation of the signal is reduced [1] because the dielectric loss produced by the ohmic mechanism is constant as a function of frequency while the conductor loss increases as the frequency increases. Therefore, the CPW on HR Si show lower losses than of the GaAs above 3 GHz. The reason why the loss characteristic of the CPW on HR Si does not change as compared to SI GaAs and quartz from -50 °C to 50 °C is because the effective ohmic loss is insensitive to temperature in this range. The effective ohmic loss is affected by temperature when the intrinsic carrier concentration becomes a significant percentage (> 25 %) of the doped carrier concentration. For the HR Si substrate under study, the temperature at which the intrinsic carrier concentration is 25 % or more of the doped carrier concentration is 80 °C. The effective ohmic loss has a two fold dependency on temperature. First, the bulk resistivity is reduced due to the increment of the intrinsic carriers. Second, the deep depletion width (> 10 µm) underneath the metal is reduced due to increment of intrinsic carrier concentration. These results are reflected on Fig. 2, which shows the measured attenuation of the CPW on various substrates at 100 °C. The attenuation of the CPW on HR Si is greater than that of GaAs up to 6 GHz. Also, the difference in attenuation between the CPW on HR Si and on SI GaAs, in Fig. 2, is reduced at higher frequencies. The measured attenuation of the CPW on HR Si, SI GaAs, and quartz are measured at 150 °C and shown on Fig. 3. At 150 °C, the attenuation of the CPW on the HR Si is dominated by the dielectric losses. The concentration of intrinsic carriers has dropped the substrate resistivity below 100 Ω-cm.

The measured unloaded quality factor (Q) of the meander structure is plotted on Figs. 4 through 5 at 100 °C and at 150 °C respectively. The measured Q of the meander on HR Si is comparable to the Q of the meander on SI GaAs up to 100 °C. At 150 °C, the measured Q of the meander on HR Si is lower than that of the meander on SI GaAs.

The other factor that can affect the losses of the CPW and the meander structure on HR Si is the DC bias which is also investigated in this paper. The depletion width impacts the effective ohmic loss. Fig. 6 shows the attenuation of the CPW on HR Si as a function of frequency at various bias settings at a 25 °C. Fig. 6 indicates that there is no change in the attenuation on the CPW due to the change of bias. The same behavior was observed at -50, -25, 0, and 50 °C. At 100 °C, it was observed that the bias on the line has a small effect on the losses. Fig. 7 shows that the attenuation at 10 volts is lower than the attenuation at -10 volts. In Fig. 8, the effect of the bias on the losses of the CPW is more pronounced at 150 °C. The measured attenuation at 10 and 3 volts is lower than the measured attenuation at 0, -3, and -10 volts. The results of Figs. 6 through 8 can be explained as follows: 1) While the depletion region under the center conductor is significantly reduced at forward bias, the depletion region under the ground planes increases; therefore, there is no an apparent net change in losses. Any change is within the noise level. 2) As the temperature increases, the depletion width decreases. The change in attenuation due to the applied bias is consistent. Positive bias on the conductor produces lower losses since the depletion area under the center conductor is smaller than the depletion area under the ground planes.

The same attenuation behavior observed in the CPW measurement on HR Si due to change in bias is observed for the meander structure on HR Si. Fig. 9 shows the measured Q of the meander as a function of frequency at 100 °C with -10, -3, 0, 3, and 10 volts bias. Fig. 9 indicates that DC bias has a second order effect in the Q of the meander. Also, there was no noticeable change due to bias at the lower temperatures settings (0 °C, -25 °C, and -50 °C). At 150 °C, the measured Q of the meander is affected by the applied bias (see Fig. 10).

CONCLUSIONS

The loss characteristics of high resistivity (> 3 k Ω-cm) Si were investigated over a wide range of temperature (150 °C to -50 °C) and a wide range of DC bias (-10 to 10 volts). The results are consistent with semiconductor and metal physics and microwave concepts. Measurements on coplanar structures on HR Si, CPW and meander, show no dependency on applied DC bias in the attenuation constant nor the unloaded Q up to 50 °. Also, the measured results of the comparative study shows that the structures on HR Si have comparable loss performance to the structures on GaAs up to temperatures of 100 °C. These results demonstrate the feasibility and practical applicability of using high resistivity Si as a microwave substrate.

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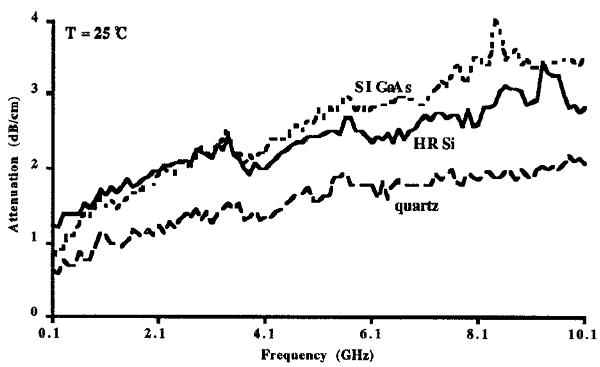

Fig. 1. Measured attenuation vs. frequency of CPW on various substrates at 25 °C.

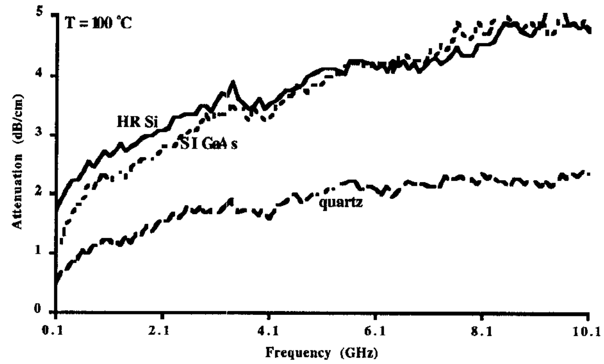

Fig. 2. Measured attenuation vs. frequency of CPW on various substrates at 100 °C.

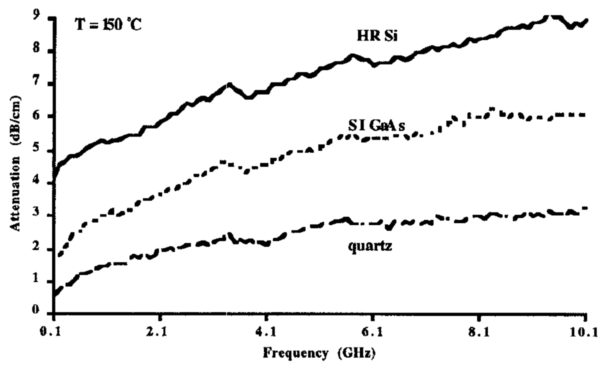

Fig. 3. Measured attenuation vs. frequency of CPW on various substrates at 150 °C.

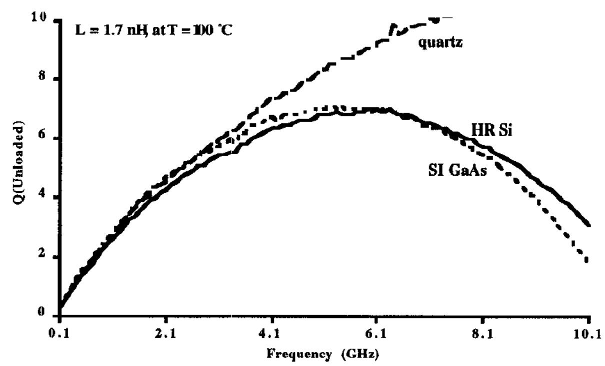

Fig. 4. Measured unloaded Q vs. frequency of meander on various substrates at 100 °C.

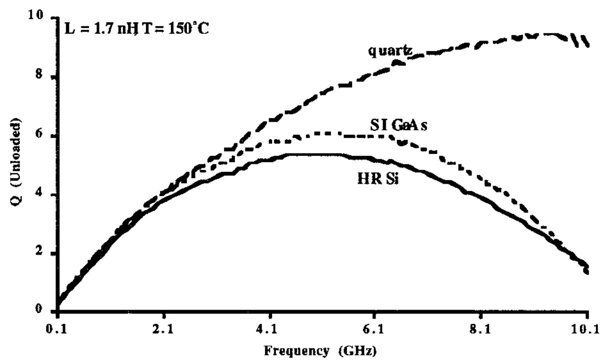

Fig. 5. Measured unloaded Q vs. frequency of meander on various substrates at 150 °C

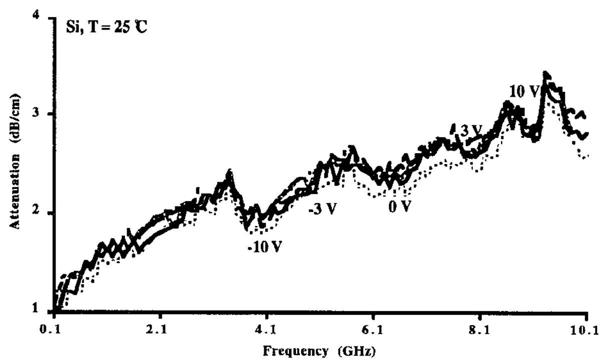

Fig. 6. Measured attenuation vs. frequency of CPW on HR Si at various bias conditions at 25 °C.

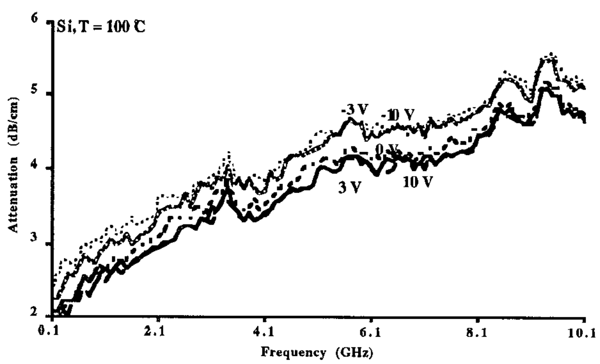

Fig. 7. Measured attenuation vs. frequency of CPW on HR Si at various bias conditions at 100 °C.

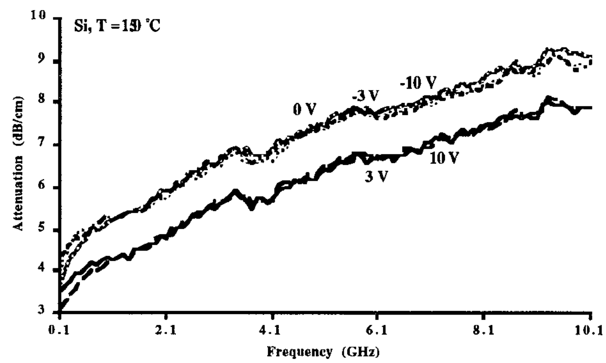

Fig. 8. Measured attenuation vs. frequency of CPW on HR Si at various bias conditions at 150 °C.

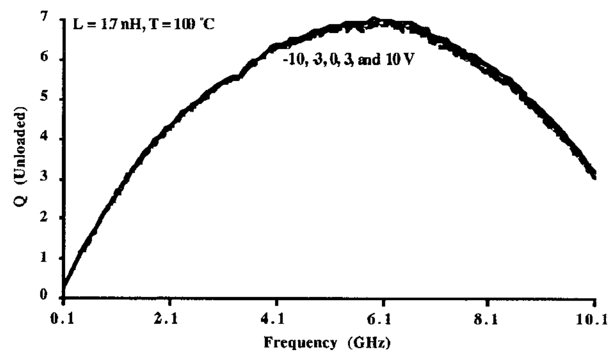

Fig. 9. Measured unloaded Q vs. frequency of meander on HR Si at various bias conditions at 100 °C.

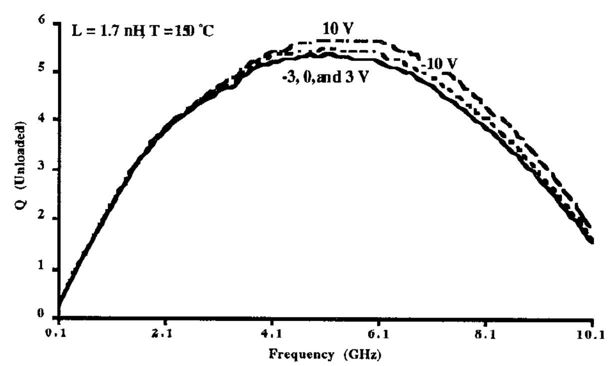

Fig. 10. Measured unloaded Q vs. frequency of meander on HR Si at various bias conditions at 150 °C.